Introduction

- Most embedded systems use only the memory built-in to the microcontroller.
- Memory interfacing and bus timing is important to understanding internal microcontroller architecture.
- Sometimes internal memory is insufficient, and external memory is needed.
- External devices can be interfaced using memory-mapped I/O.
Memory-Mapped I/O

Isolated I/O
### Expanded Mode

- **6811/6812**
- **R/W**
- **A15-A0**
- **D7-D0**

<table>
<thead>
<tr>
<th>Select</th>
<th>R/W</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Off</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Off</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Write</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Read</td>
</tr>
</tbody>
</table>

**RAM Control signals**

**Address D7-D0**

### Multiplexed Address and Data Lines

- **MC9S12C32** Bus master
- **AD15-AD0**
- **FlipFlop**
- **Two 74FCT374’s**

**RAM Address decoder**

**RAM SelectRAM**

**I/O Address decoder**

**I/O SelectI/O**

**ROM Address decoder**

**ROM SelectROM**
Full-Address Decoding

- *Slave* selected only when slave's address is on the bus.
- Design using the following steps:
  - Write specified address using 0,1,X:
    $0100,00XX,XXXX,XXXX$ for 1K RAM at $4000$-$43FF$
  - Write equation using all 0s and 1s:
    \[
    select = \overline{A_{15}} \cdot A_{14} \cdot \overline{A_{13}} \cdot \overline{A_{12}} \cdot A_{11} \cdot A_{10}
    \]
  - Build circuit using gates.

Address Decoder for 1K RAM at $4000$-$43FF$
Minimal-Cost Address Decoding

- Use don’t cares for unspecified addresses to simplify.
- Example:

<table>
<thead>
<tr>
<th>RAM</th>
<th>$0000 to $0FFF</th>
<th>Input</th>
<th>$5000</th>
<th>Output</th>
<th>$5001</th>
</tr>
</thead>
<tbody>
<tr>
<td>4K RAM</td>
<td>0000,XXXX,XXXX,XXXX</td>
<td>0101,0000,0000,0000</td>
<td>0101,0000,0000,0001</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16K ROM</td>
<td>$C000 to $FFFF</td>
<td>11XX,XXXX,XXXX,XXXX</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RAM A15 A14</th>
<th>A0</th>
<th>ROM A15 A14</th>
<th>A0</th>
<th>Input A15 A14</th>
<th>A0</th>
<th>Output A15 A14</th>
<th>A0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0</td>
<td>0</td>
<td>0 0 0 0</td>
<td>0</td>
<td>0 0 0 0</td>
<td>0</td>
<td>0 0 0 0</td>
<td>0</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>X</td>
<td>0 1 0 0</td>
<td>X</td>
<td>0 1 0 0</td>
<td>X</td>
<td>0 1 0 0</td>
<td>X</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>X</td>
<td>1 1 0 0</td>
<td>X</td>
<td>1 1 0 0</td>
<td>X</td>
<td>1 1 0 0</td>
<td>X</td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>X</td>
<td>1 0 1 0</td>
<td>X</td>
<td>1 0 1 0</td>
<td>X</td>
<td>1 0 1 0</td>
<td>X</td>
</tr>
</tbody>
</table>
An Address Decoder

A15
A14
A0

ROM select
RAM select
Output select
Input select

74HC04
74HC11

Karnaugh Maps

Cheaper
A15 A14 A0
0 0 0
0 1 In Out
1 1 ROM ROM
1 0 X X

Safer
A15 A14 A0
0 0 0
0 1 In Out
1 1 ROM ROM
1 0 X X

Expandable
A15 A14 A0
0 0 0
0 1 In Out
1 1 ROM ROM
1 0 X X
Special Cases

- Size of the memory is not a power of 2.
  - 20K RAM with address range $0000$ to $4FFF$
    - $00XX,XXXX,XXXX,XXXX$  Range $0000$ to $3FFF$
    - $0100,XXXX,XXXX,XXXX$  Range $4000$ to $4FFF$
- Start address divided by memory size not an integer.
  - 32K RAM with address range $2000$ to $9FFF$
    - $001X,XXXX,XXXX,XXXX$  Range $2000$ to $3FFF$
    - $01XX,XXXX,XXXX,XXXX$  Range $4000$ to $7FFF$
    - $100X,XXXX,XXXX,XXXX$  Range $8000$ to $9FFF$

Programmable Address Decoder

<table>
<thead>
<tr>
<th>In</th>
<th>Mn</th>
<th>An</th>
<th>Vn</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Timing Intervals

\[ (\uparrow Y, \downarrow Y) = (\downarrow A, \uparrow A) + 10 \]
\[ (\uparrow Y, \downarrow Y) = (\downarrow A, \uparrow A) + [5, 15] \]
\[ (\uparrow Y, \downarrow Y) = (\downarrow A + [8, 15], \uparrow A + [5, 12]) \]

Available and Required Time Intervals

\[ DA = (\downarrow G^* + [10, 20], \uparrow G^* + [0, 15]) \]
\[ DA = (\downarrow G^* + 20, \uparrow G^*) \text{ worst-case} \]
\[ DR = (\uparrow Clk - 30, \uparrow Clk + 5) \]
### Timing Diagrams

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>The input must be valid</td>
<td>The output will be valid</td>
</tr>
<tr>
<td></td>
<td>If the input were to fall</td>
<td>Then the output will fall</td>
</tr>
<tr>
<td></td>
<td>If the input were to rise</td>
<td>Then the output will rise</td>
</tr>
<tr>
<td>[\text{xxxxx}]</td>
<td>Don't care, it will work regardless</td>
<td>Don't know, the output value is indeterminate</td>
</tr>
<tr>
<td>[\text{---}]</td>
<td>Nonsense</td>
<td>High impedance, tristate, HiZ, Not driven, floating</td>
</tr>
</tbody>
</table>

### Example Timing Diagrams

![Timing Diagrams](image)
Read Cycle Circuit

Microcomputer

D7-D0

Slave1 data

G1

Slave2 data

G2

Slave3 data

G3

Data bus

Write Cycle Circuit

Microcomputer

D7-D0

Slave1 data

C1

Slave2 data

C2

Slave3 data

C3

Data bus
Synchronous Bus Timing

Synchronized read cycle

E
\bar{G}_1
D7-D0

Synchronized write cycle

E
C_1
D7-D0

Partially Asynchronous Bus Timing

(6809/680x0/x86)

E
Q
MRDY

Normal
Stretched
Normal

200ns

200ns
Fully Asynchronous Read Cycle

By master
I/O
REQ
By slave
ACK
Data

Fully Asynchronous Write Cycle

By master
I/O
REQ
Data
By slave
ACK
Four Types of Control Signals

Scott R. Little (Lecture 22: Memory Interfacing)
ECE/CS 5780/6780

Unsynchronized positive logic control signal
Unsynchronized negative logic control signal
Synchronized positive logic control signal
Synchronized negative logic control signal

MC9S12C32

Scott R. Little (Lecture 22: Memory Interfacing)  ECE/CS 5780/6780  26 / 40
### MC9S12C32 Modes of Operation

<table>
<thead>
<tr>
<th>BKGD</th>
<th>MODB</th>
<th>MODA</th>
<th>Description</th>
<th>Port A</th>
<th>Port B</th>
<th>MODx write</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Special</td>
<td>In/Out</td>
<td>In/Out</td>
<td>Write anytime, not peripheral</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Emulation</td>
<td>A15-A8/</td>
<td>A7-A0</td>
<td>Cannot change</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Exp. narrow</td>
<td>D7-D0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Special test</td>
<td>A15-A8/</td>
<td>A7-A0</td>
<td>Write anytime, not peripheral</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Exp. narrow</td>
<td>D15-D8</td>
<td>D7-D0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Emulation</td>
<td>A15-A8/</td>
<td>A7-A0</td>
<td>Cannot change</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Exp. wide</td>
<td>D15-D8</td>
<td>D7-D0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Normal</td>
<td>In/Out</td>
<td>In/Out</td>
<td>Write once, Norm exp N/W</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Normal</td>
<td>A15-A8/</td>
<td>A7-A0</td>
<td>Cannot change</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Exp. narrow</td>
<td>D7-D0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Peripheral</td>
<td>——</td>
<td>——</td>
<td>Cannot change</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Normal</td>
<td>A15-A8/</td>
<td>A7-A0</td>
<td>Cannot change</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Exp. wide</td>
<td>D15-D8</td>
<td>D7-D0</td>
<td></td>
</tr>
</tbody>
</table>
MC9S12C32 Expanded Mode Bus Timing

R/W LSTRB

Read
AD15-AD0

Write
AD15-AD0

Address Latch for MC9S12C32
General Approach to Memory Interfacing

Wide Expanded Mode
8K RAM Read Timing

8K RAM Write Timing
8K RAM Write Timing

\[ \begin{align*}
\text{Adv} & : A_{12}-A_0 \\
\text{AdN} & : XXXX \\
W & : XXXX \\
E_1 & \\
D_7-D_0 & : XXXX
\end{align*} \]

\[ t_{DVWH} = 60 \quad t_{WHDX} = 0 \]

Write data required

8K RAM Interface ($8000$-$9FFF$)

\[ \begin{align*}
\text{MC9S12C32} & : D_{7}-D_{0} \\
74FCT374 & : A_{15} \\
74FCT139 & : A_0 \quad A_1 \quad A_2 \quad A_3 \\
\text{MCM60L64} & : D_{Q7}-D_{Q0} \\
E_1 & \\
A_{12}-A_8 & \\
E_2 & \\
W & \\
G & \\
A_7-A_0 & \\
\end{align*} \]
8K RAM Interface Read Timing

8K RAM Interface Write Timing
Dynamic RAM (DRAM)

<table>
<thead>
<tr>
<th>DRAMs</th>
<th>SRAMs</th>
</tr>
</thead>
<tbody>
<tr>
<td>High density</td>
<td>Low density</td>
</tr>
<tr>
<td>One xtor, one cap./bit</td>
<td>3-4 xtors/bit</td>
</tr>
<tr>
<td>Slower</td>
<td>Faster</td>
</tr>
<tr>
<td>High fixed cost (refresh)</td>
<td>Low fixed cost (address decoder)</td>
</tr>
<tr>
<td>Low incremental cost</td>
<td>Higher incremental cost</td>
</tr>
<tr>
<td>Address multiplexing</td>
<td>Direct addressing</td>
</tr>
</tbody>
</table>