Introduction

- Most embedded systems use only the memory built-in to the microcontroller.
- Memory interfacing and bus timing is important to understanding internal microcontroller architecture.
- Sometimes internal memory is insufficient, and external memory is needed.
- External devices can be interfaced using memory-mapped I/O.

Memory-Mapped I/O

Isolated I/O
### Expanded Mode

**Diagram**

```
+---+ +---+ +---+ +---+ +---+
| E | R/W | A15-A0 | D7-D0 |
+---+ +---+ +---+ +---+ +---+
    |       |       |       |
    |       |       |       |
    |       |       |       |
    | Select | R/W | Function |
    | 0       | 0   | Off     |
    | 0       | 1   | Off     |
    | 1       | 0   | Write   |
    | 1       | 1   | Read    |
```

### Full-Address Decoding

- **Slave** selected only when slave’s address is on the bus.
- Design using the following steps:
  - Write specified address using 0,1,X:
    - $0100,00XX,XXXX,XXXX$ for 1K RAM at $4000$-$43FF$
  - Write equation using all 0s and 1s:
    \[
    \text{select} = \overline{A15} \cdot A14 \cdot A13 \cdot A12 \cdot A11 \cdot A10
    \]
- Build circuit using gates.
An Address Decoder for I/O Device at $5500$

- **Use don't cares for unspecified addresses to simplify.**
- **Example:**
  - 4K RAM: $0000$ to $0FFF$  $0000, XXXX, XXXX, XXXX$
  - Input: $5000$  $0101, 0000, 0000, 0000$
  - Output: $5001$  $0101, 0000, 0000, 0001$
  - 16K ROM: $C000$ to $FFFF$  $11XX, XXXX, XXXX, XXXX$

---

Minimal-Cost Address Decoding

- **Use don't cares for unspecified addresses to simplify.**
- **Example:**
  - 4K RAM: $0000$ to $0FFF$  $0000, XXXX, XXXX, XXXX$
  - Input: $5000$  $0101, 0000, 0000, 0000$
  - Output: $5001$  $0101, 0000, 0000, 0001$
  - 16K ROM: $C000$ to $FFFF$  $11XX, XXXX, XXXX, XXXX$

---

An Address Decoder

Karnaugh Maps

- **Cheaper**
  - A15 A14
  - $00$ 0
  - $01$ In Out
  - $11$ ROM ROM
  - $10$ XX XX

- **Safer**
  - A15 A14
  - $00$ 0
  - $01$ In Out
  - $11$ ROM ROM
  - $10$ XX XX

- **Expandable**
  - A15 A14
  - $00$ 0
  - $01$ In Out
  - $11$ ROM ROM
  - $10$ XX XX
Special Cases

- Size of the memory is not a power of 2.
  - 20K RAM with address range $0000$ to $4FFF$
    - $00XX,XXXX,XXXX,XXXX$ Range $0000$ to $3FFF$
    - $0100,XXXX,XXXX,XXXX$ Range $4000$ to $4FFF$
- Start address divided by memory size not an integer.
  - 32K RAM with address range $2000$ to $9FFF$
    - $001X,XXXX,XXXX,XXXX$ Range $2000$ to $3FFF$
    - $01XX,XXXX,XXXX,XXXX$ Range $4000$ to $7FFF$
    - $100X,XXXX,XXXX,XXXX$ Range $8000$ to $9FFF$

Timing Intervals

\[
(\uparrow Y, \downarrow Y) = (\downarrow A, \uparrow A) + 10 \\
(\uparrow Y, \downarrow Y) = (\downarrow A, \uparrow A) + [5, 15] \\
(\uparrow Y, \downarrow Y) = (\downarrow A + [8, 15], \uparrow A + [5, 12])
\]
### Timing Diagrams

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>The input must be valid</td>
<td>The output will be valid</td>
</tr>
<tr>
<td></td>
<td>If the input were to fall</td>
<td>Then the output will fall</td>
</tr>
<tr>
<td></td>
<td>If the input were to rise</td>
<td>Then the output will rise</td>
</tr>
<tr>
<td></td>
<td>Don’t care, it will work regardless</td>
<td>Don’t know, the output value is indeterminate</td>
</tr>
<tr>
<td></td>
<td>Nonsense</td>
<td>High impedance, tristate, HiZ, Not driven, floating</td>
</tr>
</tbody>
</table>

### Example Timing Diagrams

#### Read Cycle Circuit

- Microcomputer to Master 1:
  - D7-D0
  - Slave1 data
- Microcomputer to Master 2:
  - D7-D0
  - Slave2 data
- Microcomputer to Master 3:
  - D7-D0
  - Slave3 data

#### Write Cycle Circuit

- Microcomputer to Master 1:
  - D7-D0
  - Slave1 data
- Microcomputer to Master 2:
  - D7-D0
  - Slave2 data
- Microcomputer to Master 3:
  - D7-D0
  - Slave3 data
Synchronous Bus Timing

Partially Asynchronous Bus Timing (6809/680x0/x86)

Fully Asynchronous Read Cycle

Fully Asynchronous Write Cycle
Four Types of Control Signals

- Unsynchronized positive logic control signal
- Unsynchronized negative logic control signal
- Synchronized positive logic control signal
- Synchronized negative logic control signal

MC9S12C32 Modes of Operation

<table>
<thead>
<tr>
<th>BKGD</th>
<th>MODB</th>
<th>MODA</th>
<th>Description</th>
<th>Port A</th>
<th>Port B</th>
<th>MODx write</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Single chip</td>
<td>In/Out</td>
<td>In/Out</td>
<td>Write anytime, not peripheral</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Emulation</td>
<td>A15-A8/D7-D0</td>
<td>A7-A0</td>
<td>Cannot change</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Special test</td>
<td>A15-A8/D15-D8</td>
<td>A7-A0</td>
<td>Write anytime, not peripheral</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Emulation</td>
<td>A15-A8/D15-D8</td>
<td>A7-A0</td>
<td>Cannot change</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Normal</td>
<td>In/Out</td>
<td>In/Out</td>
<td>Write once, Norm exp N/W</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Normal</td>
<td>A15-A8/D7-D0</td>
<td>A7-A0</td>
<td>Cannot change</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Peripheral</td>
<td>–</td>
<td>–</td>
<td>Cannot change</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Normal</td>
<td>A15-A8/D15-D8</td>
<td>A7-A0</td>
<td>Cannot change</td>
</tr>
</tbody>
</table>

MC9S12C32 Clock Circuit
MC9S12C32 Expanded Mode Bus Timing

Address Latch for MC9S12C32

General Approach to Memory Interfacing

Wide Expanded Mode
### 8K RAM Read Timing

- A12-A0
- \( t_{AVQV} = 150 \)
- \( t_{AXQX} = 20 \)
- \( t_{E1HQZ} = 0 \)
- D7-D0
- Read data available

### 8K RAM Write Timing

- A12-A0
- \( t_{DVWH} = 60 \)
- \( t_{WHDX} = 0 \)
- D7-D0
- Write data required

### 8K RAM Interface ($8000$-$9FFF$)

- MC9S12C32
- 74FCT139
- 74FCT134
- MCM60L64
8K RAM Interface Read Timing

8K RAM Interface Write Timing

8K by 16-bit RAM Interface

Dynamic RAM (DRAM)

<table>
<thead>
<tr>
<th>DRAMs</th>
<th>SRAMs</th>
</tr>
</thead>
<tbody>
<tr>
<td>High density</td>
<td>Low density</td>
</tr>
<tr>
<td>One xtor, one cap./bit</td>
<td>3-4 xtors/bit</td>
</tr>
<tr>
<td>Slower</td>
<td>Faster</td>
</tr>
<tr>
<td>High fixed cost (refresh)</td>
<td>Low fixed cost (address decoder)</td>
</tr>
<tr>
<td>Low incremental cost</td>
<td>Higher incremental cost</td>
</tr>
<tr>
<td>Address multiplexing</td>
<td>Direct addressing</td>
</tr>
</tbody>
</table>