CS/EE 5830/6830 VLSI Architecture
CAD Assignment #4
Due Thursday Mar 3rd, 5:00pm

This assignment will consist of all problems from the book – no Cadence this time. CAD5 will be a return to Cadence…

You can use handin to the CAD4 assignment directory, or turn this in on paper.

1. Problem 3.3 – Use the following table for delays in the FA and HA cells:

	FA		HA	
To / From	**Cout**	**S**	**Cout**	**S**
(x,y)		2	0.7	1.2
x	2			
y	1.5			
Cin	1	1.2		

For part a) use an array of [5 :2] adders as described in the problem. For part b) with the [3:2] adders the right way to think about this is to use one row of [3:2] to do a carry-save reduction for 3 arguments, then another row of [3:2] adders to take the carry save sum and add one more vector, then another row like that. So, it's like iterative carry-save summation. "Compare" means to compare the delay of the worst case (critical) paths of the two approaches and also count the number of FA and HA cells used.

2. Problem 3.5 – pretty straightforward...
3. Problem 3.8 – pretty straightforward…
4. Problem 3.9 - pretty straightforward...

5. Problem 3.13 – Use the same delay table as in 3.3 to compute the delays (for the "compare" part). For part a) you should think about this as using the [5:2] adders in the first row, and the [4:2] adders in the second. Compare delays and also number of FA and HA cells needed.

6. Problem 3.22 – CRA is Carry Ripple Adder. CPA is Carry Propagate Adder (the class of adders that propagates carries).

7. Problem 3.24 – similar to example 3.3 in the book.