Designing the first five cells in your library
  - Multiple cell views
- ELC library characterizer
- Abstract generator
- Synopsys database generation
  - Using the cells in synthesis

CS/ECE 6710 Tool Suite

Verilog sim

Behavioral Verilog

Synopsys Design Compiler

Your Library

CCAR AutoRouter

Cadence EDI

Circuit Layout

LVS

Layout-XL

Behavioral Verilog

Structural Verilog

Verilog sim

Cadence Virtuoso Layout

Cadence Composer Schematic
Start with Cells

Layout View
Behavioral View

module NAND2X1 (Y, A, B);
    output Y;
    input A;
    input B;

    nand_10(Y, A, B);

    specify
        (A == Y) = (1, 0, 1, 0);
        (B == Y) = (1, 0, 1, 0);
    endspecify

endmodule

Single Schematic with All Cells
Single Schematic with All Cells

Create Netlist of that Cell
Create Netlist of that Cell

```
// Generated for: spectre
// Generated on: Oct 10 13:35:45 2013
// Design library name: Lib6710_00
// Design cell name: ss-test
// Design view name: schematic
simulator lang=spectre
global 0 vdd
include 'namesrc/family/real_common/local/class/6710/ssa/spectre/ssa.scs'
library name: Lib6710_00
// Cell name: INVX1
// View name: nmos_sch
include ENVIY A Y lnk_inh_bn_net0
M1 (Y A vdd node0) and06 w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \ 
  pd=9u m=1 region=sgt
M2 (Y A vdd node0) and06 w=3u l=600n as=2.25e-12 ad=2.25e-12 \ 
  ps=9u pd=9u m=1 region=sgt
ends INVX1
// End of schematic definition.
// Library name: Lib6710_00
// Cell name: INVX1
// View name: nmos_sch
include ENVIY A Y lnk_inh_bn_net0
M1 (Y B vdd node0) and06 w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \ 
  pd=9u m=1 region=sgt
M2 (Y B vdd node0) and06 w=3u l=600n as=2.25e-12 ad=2.25e-12 \ 
  ps=9u pd=9u m=1 region=sgt
M2 (Y A net12 inh_inh_bn) am06n w=3u l=600n as=4.5e-12 ad=4.5e-12 \ 
  ps=9u pd=9u m=1 region=sgt
ends INVX1
include ENVIY A Y lnk_inh_bn_net0
M1 (Y A vdd node0) am06p w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \ 
  pd=9u m=1 region=sgt
M2 (Y A vdd node0) am06p w=3u l=600n as=2.25e-12 ad=2.25e-12 \ 
  ps=9u pd=9u m=1 region=sgt
ends INVX1
include ENVIY A Y lnk_inh_bn_net0
M1 (Y B vdd node0) am06p w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \ 
  pd=9u m=1 region=sgt
M2 (Y A net12 inh_inh_bn) am06n w=3u l=600n as=4.5e-12 ad=4.5e-12 \ 
  ps=9u pd=9u m=1 region=sgt
ends INVX1
```

Convert to ELC format

```
sp2elc foo.scs dut.scs
```
Run ELC

- **Encounter Library Characterizer**
  - Figures out what each cell is (logic)
  - Generates test inputs for Spectre
  - Runs Spectre
  - Checks output and extracts timings
  - Formats the output in .alf format

```
cad-elc -S step1
```

Results from ELC step1

```
elc> db_gate
----------------------------------------
    DESIGN : INVX1
----------------------------------------
    NOT ( Y, A );
----------------------------------------
    DESIGN : NAND2X1
----------------------------------------
    NAND2 ( Y, A, B );
----------------------------------------
    DESIGN : NORX1
----------------------------------------
    NOR ( Y, A, B );
```

Lots of text missing from these highlights…
Results from ELC step 1

```plaintext
-------------
DESIGN : MMO201
-------------

/* PART DEFINITION */

INPUT A (A)
INPUT B (B);
OUTPUT Y (Y);
SUPPLY VDD (VDD);
SUPPLY GND (GND);
SUPPLY IML (IML);
SUPPLY IMH (IMH);
SUPPLY IOM (IOM);
SUPPLY IHE (IHE);

/* INSTANCES */

MMO (Y, A, B);
END_OF_DESIGN

-------------
DESIGN : MM021
-------------

/* PART DEFINITION */

INPUT A (A)
```
Results from ELC step2

cad-elc -S step2

elc> db_spice -s spectre -p typical -keep_log

<table>
<thead>
<tr>
<th>DESIGN</th>
<th>PROCESS</th>
<th>#ID</th>
<th>STATUS</th>
<th>IPDB</th>
</tr>
</thead>
<tbody>
<tr>
<td>INVX1</td>
<td>typical</td>
<td>D0000</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>INVX1</td>
<td>typical</td>
<td>D0001</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>D0002</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>D0003</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>D0004</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>D0005</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>D0006</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>D0007</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>2</td>
<td>2</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>D0000</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>D0001</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>D0002</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>D0003</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>D0004</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>D0005</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>D0006</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>D0007</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NAND2X1</td>
<td>typical</td>
<td>8</td>
<td>8</td>
<td>foo</td>
</tr>
<tr>
<td>NOR2X1</td>
<td>typical</td>
<td>D0000</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NOR2X1</td>
<td>typical</td>
<td>D0001</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
<tr>
<td>NOR2X1</td>
<td>typical</td>
<td>D0002</td>
<td>SIMULATE</td>
<td>foo</td>
</tr>
</tbody>
</table>

Lots of text missing from these highlights…
Results from ELC step2

- Total Simulation: 20
- Total Passed: 20 (100.00%)
- Total Failed: 0 (0.00%)

Results from ELC step3

elc> db_output -report foo.alf.rep -alf foo.alf -p typical
NAND2X1 typical   2013-10-10 13:55:23 (2013-10-10 19:55:23 GMT) 8 (100%)
NOR2X1  typical   2013-10-10 13:55:23 (2013-10-10 19:55:23 GMT) 8 (100%)
elc> db_verilog -r foo.v
Reading: foo.ipdb/INVX1.design

DESIGN: INVX1

Reading: foo.ipdb/NAND2X1.design

DESIGN: NAND2X1

...
Results from cad-alf2lib

CELL INVX1:
   now reading
   now converting
   ***** successful *****
CELL NAND2X1:
   now reading
   now converting
   ***** successful *****
...  
CELL TIEHI:
   now reading
   now converting
   ***** successful *****
CELL TIELO:
   now reading
   now converting
   ***** successful *****
---
Total : 5 cells ( successful : 5  failed : 0 )

Lots of text missing from these highlights…

Changing Names

- The ELC scripts make a library named “foo”
- Probably good to rename it Lib6710_00
  - Rename foo.lib to Lib6710_00.lib
    - You have to modify the library name inside the .lib file
  - Rename foo.v to Lib6710_00.v
  - You generate Lib6710_00.db from Lib6710_00.lib
Changing foo.lib to Lib6710_00.lib

---

Changing foo.lib to Lib6710_00.lib

---
Lib6710_00.lib

```c
/* -- -- -- -- -- -- -- -- -- *
 * Design: INVX1 *
 * Version: 1.0

Cell (INVX1) {
    area : 0.6;
    cell_leakage_power : 0.003784;
    rail_connection{ GND, RAIL_00 }; // 0.8V
    rail_connection{ INV_INH_00, RAIL_INV_INH_00 }; // 0.6V
    rail_connection{ VDD, RAIL_VDD }; // 0.9V
    rail_connection{ NET0, RAIL_NET0 }; // 2.45V

    pnm(A) {
        direction : input;
        input_signal_level : RAIL_VDD;
        capacitance : 0.007467;
        rise_capacitance : 0.007467;
        fall_capacitance : 0.007467;
        rise_capacitance_range ( 0.007467, 0.007467 );
        fall_capacitance_range ( 0.007467, 0.007467 );
        max_transition : 1.2;
    }

    pnf(Y) {
        direction : output;
        output_signal_level : RAIL_VDD;
        capacitance : 0;
    }
}
```

```
Lib6710_00.lib

```c
rise_transition(delay_template_5x5) {
    index_1 (0.06, 0.18, 0.42, 0.6, 1.2*);
    index_2 (0.025, 0.65, 0.1, 0.3, 0.6*);
    values ( \n    "0.190512, 0.346297, 0.638393, 1.027905, 3.613495", \n    "0.397985, 0.394239, 0.639005, 1.028325, 3.621654", \n    "0.201406, 0.371036, 0.642082, 1.027740, 3.613020", \n    "0.295946, 0.422836, 0.665162, 1.028375, 3.616693", \n    "0.442069, 0.560119, 0.794422, 1.037447, 3.616993" );
}
```

```
cell_fall(delay_template_5x5) {
    index_1 (0.06, 0.18, 0.42, 0.6, 1.2*);
    index_2 (0.025, 0.65, 0.1, 0.3, 0.6*);
    values ( \n    "0.32896, 0.541746, 0.965774, 2.670291, 5.197913", \n    "0.39724, 0.600395, 1.035125, 2.74489, 5.26392", \n    "0.545981, 0.753354, 1.176309, 2.069309, 5.396682", \n    "0.660319, 0.864524, 1.281045, 2.79966, 5.580086", \n    "1.06926, 1.247936, 1.655945, 3.333276, 5.85147" );
}
```

```
fall_transition(delay_template_5x5) {
    index_1 (0.06, 0.18, 0.42, 0.6, 1.2*);
    index_2 (0.025, 0.65, 0.1, 0.3, 0.6*);
    values ( \n    "0.066081, 0.106452, 0.219645, 0.354424, 0.479790", \n    "0.105125, 0.140486, 0.273834, 0.407784, 0.522736", \n    "0.144179, 0.179538, 0.312886, 0.446836, 0.561788", \n    "0.183233, 0.218582, 0.351931, 0.485880, 0.600832", \n    "0.222287, 0.257631, 0.391979, 0.525929, 0.634882" );
}
```
Converting .lib to .db

[elb@lab2-12 ELC]$ syn-dc
Using setup-synopsys from S13/F13
Assuming your OS is amd64
You are now set up to run the synopsys tools.
Working directory is /home/elb/VLSI/cadence-f13/ELC

Design Compiler Graphical
  DC Ultra (TM)
  DFTMAX (TM)
Power Compiler (TM)
  DesignWare (R)
  DC Expert (TM)
  Design Vision (TM)
  HCL Compiler (TM)
  VHCL Compiler (TM)
  DFT Compiler
  Library Compiler (TM)
  Design Compiler (R)

Version G-2012.06-SP3 for RHEL64 -- Oct 23, 2012
Copyright (c) 1988-2012 Synopsys, Inc.
This software and the associated documentation are confidential and proprietary to Synopsys, Inc. Your use or disclosure of this software is subject to the terms and conditions of a written license agreement between you, your company, and Synopsys, Inc.

dc_shell> read_lib Lib6710_00.lib
Reading '/home/elb/VLSI/cadence-f13/ELC/Lib6710_00.lib' ...
Warning: Line 81, Cell 'INVX1', pin 'A', The pin 'A' does not have a internal_power group. (LBDB-607)
Information: Line 571, Cell 'TIEHI', No internal_power information for the 'TIEHI' cell. (LBDB-301)
Warning: Line 578, Cell 'TIEHI', pin 'Y', The pin 'Y' does not have a internal_power group. (LBDB-607)
Information: Line 589, Cell 'TIELO', No internal_power information for the 'TIELO' cell. (LBDB-301)
Warning: Line 596, Cell 'TIELO', pin 'Y', The pin 'Y' does not have a internal_power group. (LBDB-607)
Warning: Line 11, The 'default_fanout_load' attribute is not specified. Using 1.00. (LBDB-172)
Warning: Line 11, The 'default_input_pin_cap' attribute is not specified. Using 1.00. (LBDB-172)
Warning: Line 11, The 'default_input_pin_cap' attribute is not specified. Using 1.00. (LBDB-172)
Warning: Line 11, The 'default_output_pin_cap' attribute is not specified. Using 0.00. (LBDB-172)
Warning: Line 11, The 'default_cell_leakage_power' attribute is not specified. Using 0.00. (LBDB-172)
Warning: Line 11, The 'default_leakage_power_density' attribute is not specified. Using 0.00. (LBDB-172)
Technology library 'Lib6710_00' read successfully

Lots of text missing from these highlights...
Converting .lib to .db

```bash
dc_shell> write lib Lib6710_00 -o Lib6710_00.db
Wrote the 'Lib6710_00' library to '/home/elb/VLSI/cadence-f13/ELC/Lib6710_00.db' successfully.
```

Lots of text missing from these highlights…

Generating Abstract Views
Imported library in cad-abstract

Green checks are good!
Export Lib6710_00.lef file

Replace highlighted text with TechHeader.lef from class ELC directory

“geometry lef”
“geometry lef”

Replace highlighted text with TechHeader.lef from class ELC directory

Final CAD5 Files…

- Nine views of every cell
  - abstract, abstract.ext, abstract.pin, analog_extracted, behavioral, cmos_sch, extracted, layout, symbol
  - DRC and LVS-checked, and simulated

- Four versions of the library description
  - Lib6710_00.lib
  - Lib6710_00.db
  - Lib6710_00.v
  - Lib6710_00.lef
All Nine Views…

Test with beh2str

- `beh2str addsub.v addsub_dc.v Lib6710_00.db`

- Results in `addsub_dc.v` and `addsub_dc.v.rep`
module addsub (a, b, addnsub, result);
  input [7:0] a;
  input [7:0] b;
  output [8:0] result;
  input addnsub;
  wire n26, n27, n28, n29, n30, n31, n32, n33, n34, n35, n36, n37, n38, n39,
  n40, n41, n42, n43, n44, n45, n46, n47, n48, n49, n50, n51, n52, n53,
  n54, n55, n56, n57, n58, n59, n60, n61, n62, n63, n64, n65, n66, n67,
...
NAND2X1 U33 (.A(n26), .B(n27), .Y(result[8]));
NAND2X1 U34 (.A(b[7]), .B(n28), .Y(n27));
NAND2X1 U35 (.A(n29), .B(n30), .Y(n28));
NOR2X1 U36 (.A(n31), .B(n32), .Y(n29));
...
NOR2X1 U216 (.A(n188), .B(a[0]), .Y(n175));
NAND2X1 U217 (.A(a[0]), .B(n188), .Y(n202));
INVX1 U218 (.A(b[0]), .Y(n188));
endmodule

addsub_dc.v.rep

Operating Conditions: typical   Library: Lib6710_00
Wire Load Model Mode: top
Startpoint: b[1] (input port)
Endpoint: result[8] (output port)
Path Group: (none)
Path Type: max
Point    Incr    Path
--------------------------------------------
input external delay                     0.00       0.00 r
b[1] (in)                                0.00       0.00 r
U198/Y (NOR2X1)                          0.50       0.50 f
U194/Y (NOR2X1)                          0.36       0.86 r
...
U34/Y (NAND2X1)                          0.25      10.16 f
U33/Y (NAND2X1)                          0.24      10.40 r
result[8] (out)                          0.00      10.40 r
data arrival time                        10.40

(Path is unconstrained)
addsub_dc.v.rep

Library(s) Used:

Lib6710_00 (File: /home/elb/VLSI/cadence-f13/syn-f13/CAD5test/
Lib6710_00.db)

Number of ports: 26
Number of nets: 203
Number of cells: 186
Number of combinational cells: 186
Number of sequential cells: 0
Number of macros: 0
Number of buf/inv: 37
Number of references: 3

Summary

✦ You now have a library that is fully functional
  - BUT – only on combinational circuits
  - No DFF yet!

✦ Every step of the way requires extreme care to get things exactly right
  - No trick to finding the right answer
  - The point is to practice working with the data & tools